ATM SWITCH MODELING AND SIMULATION*

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ABSTRACT

Traffic management is increasingly becoming an important focus of study in Asynchronous Transfer Mode (ATM) networks. This is because, unlike shared-medium LAN technologies where users compete for bandwidth, ATM technology has the ability to deliver high degrees of quality of service (QoS) while simultaneously supporting multiple traffic classes on the same transmission path. In this context, *congestion control* through adequate buffering is becoming particularly significant to minimize the probability of cell loss and cell delay when multiple large traffic bursts are received concurrently at a switch.

In this paper we investigate the behavior of ATM traffic with varying buffer sizes. The impact on CLR and end-to-end delay is studied using the OPNET network modeling and simulation package from Mil3 Inc. The traffic mix consists of high priority and low priority traffic with fixed size buffers. The effect of high priority class traffic on low priority traffic is shown.

1 INTRODUCTION

The recent emergence of Asynchronous Transfer Mode (ATM) technology provides a unique opportunity to become a driving technology for high performance computing platforms, with line speeds that will scale to interfaces in the gigabit range. Unlike shared-medium LAN technologies in which users compete for bandwidth, the ATM network is capable of dynamically allocating bandwidth as a function of priority. The primary benefits that ATM technology offers over competing technologies are priority-based dynamic bandwidth allocation, the ability to intermix all classes of traffic (such as data, voice, video) with different latency and delay requirements on the same transmission and switching fabric, and the ability to support all this traffic with a guaranteed quality of service (QoS).

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An ATM network provides its users guaranteed Quality of Service (QoS). To achieve this QoS, a traffic contract is secured between the user and the network where the user informs the network of the traffic parameters and desired QoS for each direction of the requested connection upon initial set-up. Traffic management is particularly important in providing this guaranteed QoS required by the users in the ATM network.

Switch buffer architecture is an important issue because buffers are required to secure low cell-loss rate by providing a place to guard against cell loss when the switch is overloaded. The choice of buffering method as well as the size of the buffer can have a dramatic effect on the performance of a switch. If cell loss is experienced due to overflowing buffers, this will induce a degradation in the overall system performance. Large buffers may be expensive. More importantly, they may create excessive latency to delay-sensitive traffic, denying its QoS. On the other hand, small buffers may seriously penalize an application because of buffer overflows. Therefore, optimal buffer size depends on tradeoffs between a number of parameters such as throughput, end-to-end delay, and cost. However, to control or limit congestion, adequate buffering should be implemented to minimize the probability of cell loss when multiple large traffic bursts are received concurrently at a switch. This raises a number of questions: What is the optimum size of a buffer and what is the impact of cell loss and cell delay on performance due to a particular buffer size? What are the effective methods of buffer management ? Answers to these questions can be generated using simulation models.

Simulation models are useful in investigating the detailed operation of an ATM system. In this study, OPNET simulation package is used to explore the feasibility of effective buffer management control schemes to prevent congestion within the ATM switch. OPNET of Mil3 Inc. is a comprehensive development environment supporting modeling and performance evaluation of communication networks and distributed systems. It provides extensive support for developing ATM model components with the programming language called Proto-C. Since this environment provides the ability to model new, or alter the existing, communication protocols and algorithms using a high level language, a detailed ATM switch performance has been simulated under a mix of traffic patterns.

2 SIMULATION MODEL

The *OPNET* simulation package allows a hierarchical representation of the network to be studied. For this paper, the topmost layer consisted of a simple network connecting a traffic source Figure [1] to a sink Figure [2] via a central switch Figure [3]. The traffic source generates traffic of two types, high priority class “A” traffic and low priority class “D” traffic. The cells belonging to each class are appropriately marked by using the *Cell Loss Priority* bit in the ATM header. The traffic pattern we chose to study consists of an ON/OFF type of traffic. Within the ON state the packets are generated with an exponential probability distribution with a given mean. The following parameters are typical for one simulation run:

SAR rate	1222650	packets/sec
Class “D”		
call duration	2.0	sec
call wait time	1.0	sec
interarrival time	0.000028	sec
packet size	384	bits
Class “A”		
call duration	1.0	sec
call wait time	0.5	sec
inter arrival time	0.000012	sec
packet size	384	bits

The link rates have been set to 51.84 Mbits/sec, which corresponds to *STS-1*. Assuming these simulation parameters, the link utilization is 95 % if both sources are transmitting packets at the same time. Out of this, 70 % traffic is of the high priority class “A” type, while the rest is of class “D” type. The *Segmentation and Assembly Rate* has been kept very high so that there is no false traffic shaping due to the *AAL 5* layer. Since the packet size is fixed at 384 bits, segmentation is not required, and this does not introduce any error. It should be noted that the default *OPNET* traffic contract is based on the *Peak Cell Rate*, where the *PCR* is calculated as follows:

$$PCR = \frac{1.0 \times \text{packet size}}{\text{inter-arrival time} \times 384}$$

Time Interval	Class “A”	Class “D”
0 – 0.5	OFF	OFF
0.5 – 1.0	ON	OFF
1.0 – 1.5	ON	ON
1.5 – 2.0	OFF	ON
2.0 – 3.0	ON	ON
3.0 –3.5	OFF	OFF
3.5 – 4.0	ON	OFF
4.0 – 4.5	ON	ON
4.5 – 5.0	OFF	ON

Table 1: *Traffic States*

Some sample results of the average end-to-end delay are shown Figure [4]. For this case the buffer size in the switch was set to 2000 cells for call “A” and 2 cells for class “D”. As can be seen from the graph, the ON and OFF states of the two traffic sources have a clear impact on the respective end-to-end delays. The behavior of the curves is as shown in Table[1].

3 CONCLUSION

We have shown how a simulation tool like *OPNET* can be used to study sophisticated communication networks based on *ATM*. Future work would include changing the traffic contract parameters to include the average cell rate besides the peak cell rate. The existing version tends to underutilise the link. Some thought must be given on determining an appropriate SAR. Within the simulation model the SAR can be either set to equal the PCR or to some fixed value. We found that if the SAR is allowed to equal the PCR as calculated earlier, statistical variations in the traffic pattern can introduce false buffering in the SAR layer, which is not desirable in this framework.

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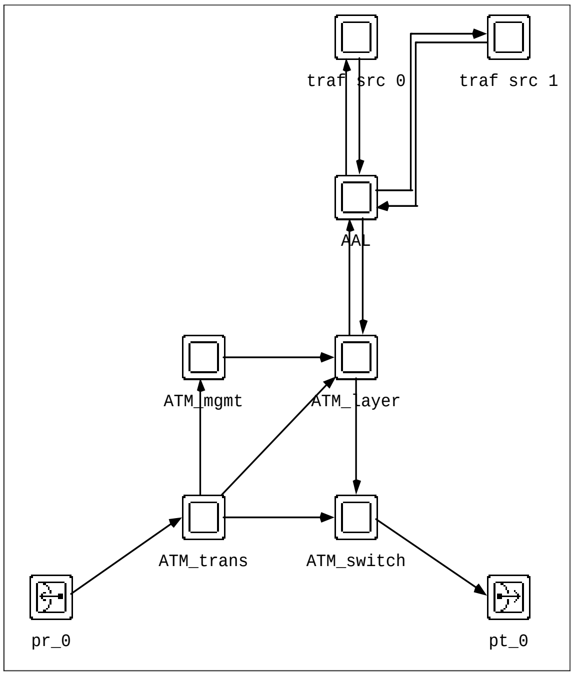

Figure 1: *Traffic Source*

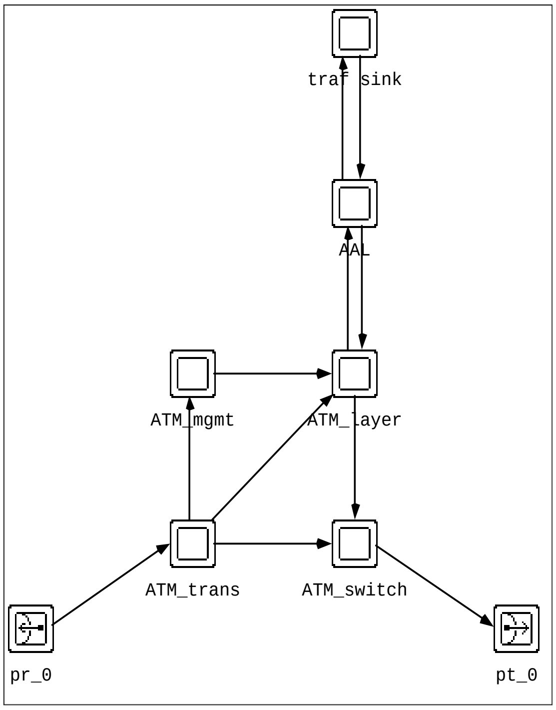

Figure 2: *Traffic Sink*

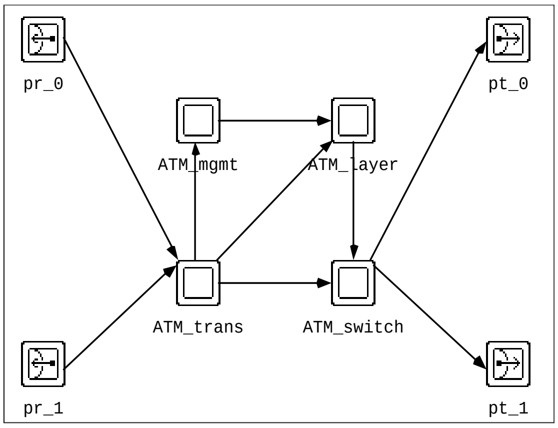

Figure 3: *Traffic Switch*

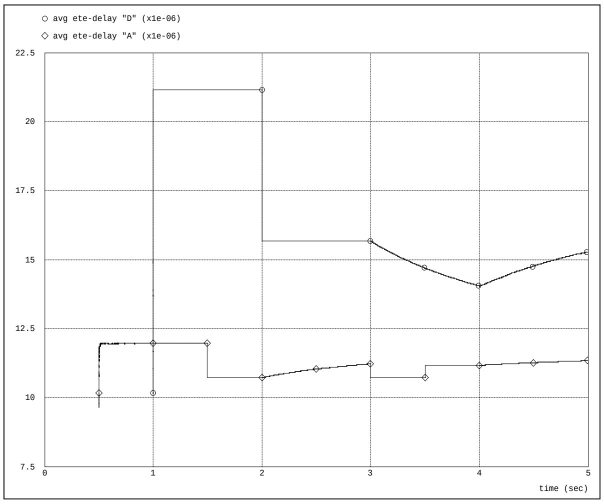

Figure 4: *End-to-end Delay*